CLAIMS

1. A ferroelectric memory device having plural memory cells each composed of a memory cell transistor and a memory cell capacitor, wherein

said respective memory cell capacitor comprises:

a lower electrode that is connected to a bit line via the memory cell transistor;

a ferroelectric layer that is formed on an upper surface of the lower electrode and has a width direction of the lower electrode as its width direction; and

an upper electrode that is formed on an upper surface of the ferroelectric layer and has a width direction of the lower electrode as its width direction,

said lower electrode of the respective memory cell capacitor is independent for each of the memory cell capacitors,

said upper electrode of the respective memory cell capacitor constitutes a plate electrode that is common to the plural memory cell capacitors, and

the width of said upper electrode is narrower than the width of the ferroelectric layer.

2. The ferroelectric memory device as defined in Claim 1 wherein

the width of the lower electrode is narrower than the width of the ferroelectric layer.

3. The ferroelectric memory device as defined in Claim 2 wherein

the width of the upper electrode and the width of the lower electrode are substantially the same, and

the position of the upper electrode in the width direction and the position of the lower electrode in the width direction substantially aligns with each other.

4. The ferroelectric memory device as defined in Claim 2 wherein

the width of the upper electrode and the width of the lower electrode are substantially the same, and

the position of the upper electrode in the width direction and the position of the lower electrode in the width direction are different from each other.

5. A ferroelectric memory device having plural memory cells each composed of a memory cell transistor and a memory cell capacitor, wherein

said respective memory cell capacitor comprises:

a lower electrode that is connected to a bit line via the memory cell transistor;

a ferroelectric layer that is formed on an upper surface of the lower electrode; and

an upper electrode that is formed on an upper surface of the ferroelectric layer,

said lower electrode of the respective memory cell

capacitor is independent for each of the memory cell capacitors,

said upper electrode of the respective memory cell capacitor constitutes a plate electrode that is common to the plural memory cell capacitors,

a position of one edge of the upper electrode substantially aligns with a position of an edge of the ferroelectric layer, and

the other edge of the upper electrode is located at an inner position with relative to the ferroelectric layer.

6. The ferroelectric memory device as defined in Claim 5 wherein

a position of one edge of the lower electrode substantially aligns with a position of one edge of the upper electrode.

7. A ferroelectric memory device having plural memory cells each composed of a memory cell transistor and a memory cell capacitor, wherein

said respective memory cell capacitor comprises:

a lower electrode that is connected to a bit line via the memory cell transistor;

a ferroelectric layer that is formed on an upper surface of the lower electrode; and

an upper electrode that is formed on an upper surface of the ferroelectric layer,

said lower electrode of the respective memory cell

capacitor is independent for each of the memory cell capacitors,

said upper electrode of the respective memory cell capacitor constitutes a plate electrode that is common to the plural memory cell capacitors,

a position of one edge of the upper electrode substantially aligns with a position of an edge of the ferroelectric layer,

the other edge of the upper electrode is located at an inner position with relative to the ferroelectric layer, and

one edge of the lower electrode is located at an inner position with relative to the ferroelectric layer, and a position of the other edge of the lower electrode substantially aligns with a position an edge of the ferroelectric layer.

8. The ferroelectric memory device as defined in Claim 1 wherein

the lower electrode has a groove-type structure.

9. The ferroelectric memory device as defined in Claim 8 wherein

a groove formed in the lower electrode extends along a direction that is parallel to the direction along which the upper electrode extends.

10. The ferroelectric memory device as defined in Claim 8 wherein

a direction along which the groove formed in the lower electrode extends is perpendicular to a direction along which

the upper electrode extends.

11. A ferroelectric memory device having plural memory cells each composed of a memory cell transistor and a memory cell capacitor, wherein

said respective memory cell capacitor comprises:

a lower electrode that is connected to a bit line via the memory cell transistor;

a ferroelectric layer that is formed on an upper surface of the lower electrode; and

an upper electrode that is formed on an upper surface of the ferroelectric layer,

said lower electrode of the respective memory cell capacitor is an electrode having a groove-type structure that is independent for each memory cell capacitor, and

said upper electrode of the respective memory cell capacitor constitutes a plate electrode that is common to the plural memory cell capacitors.

12. The ferroelectric memory device as defined in Claim 11 wherein

a groove formed in the lower electrode extends along a direction that is parallel to the direction along which the upper electrode extends.

13. The ferroelectric memory device as defined in Claim 11 wherein

a groove formed in the lower electrode extends along a

direction that is perpendicular to a direction along which a upper electrode extends.

14. The ferroelectric memory device as defined in Claim 11 wherein

the lower electrode having the groove-type structure comprises:

a first lower electrode section in a planar shape that constitutes a bottom part of the groove, and

a second lower electrode section that constitutes side surface parts and circumference parts of the groove.

15. The ferroelectric memory device as defined in Claim 11 wherein

the lower electrode having the groove-type structure comprises:

a first lower electrode section that constitutes a bottom part of the groove; and

a second lower electrode section that constitutes only side surface parts of the groove.